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1. Field of the Invention The present invention relates to a method for etching a silicon substrate. 2. Description of the Background Art In semiconductor manufacturing processes, a dry etching method using a plasma is commonly used as a method for forming a fine pattern on a semiconductor substrate. The dry etching process of a substrate is classified into a batch process which processes a plurality of wafers at a time, and a single-wafer process which processes a single wafer. When performing the etching on the wafer, a mask on which a given pattern is drawn is formed on the wafer. The pattern drawn on the mask is transferred to the wafer by the use of the etching technique in order to form a

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desired pattern on the wafer. In the dry etching process, a wafer etched to a given thickness is obtained as a product. In the etching process, a polishing process is performed for finishing a wafer on which a pattern has been drawn. The polishing process is usually performed in the wet state. However, in recent years, a polishing process in the dry state has been considered. The dry polishing process is a process of removing a photoresist film used as a mask and removing oxide films from the surface of a wafer etched in the wet state by a polishing process. The polishing process of the wafer becomes less effective when an oxide film is thickened by etching in the wet state. On the other hand, when the oxide film is thickened by etching in the wet state, the dry polishing is advantageously performed because an oxide film is not removed and thus a coarse wafer surface cannot be obtained. When performing the dry polishing, a film of alumina used as a polishing cloth is formed on a polishing pad.

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The film is maintained in a constant thickness by repeatedly performing a process of attaching a wafer to the polishing pad, and a process of pressing the wafer on the polishing pad and then detaching the wafer from the polishing pad. In the polishing process, the thickness of the oxide film

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```
Query.update(query, doc, function(error) {  
  console.log("Updated doc: %s", doc._id);  
}); } else { console.log(error); } });
```

Reference link: as pre-determined by the controller 3. The control signal from the controller 3 is transmitted to the RAM 2 via the transfer channel 2a, and is input as address data to the MRAM 2. In the MRAM 2, a series of discharge pulses are applied to the MRAM memory cell 1 to store a data value. A discharge pulse train is applied at a write-enable time point T1 when the pre-determined address data is applied to the RAM 2 via the transfer channel 2a. The state of the MRAM cell 1 is compared to the comparison reference voltage  $V_{t0}$  on the basis of the change of the